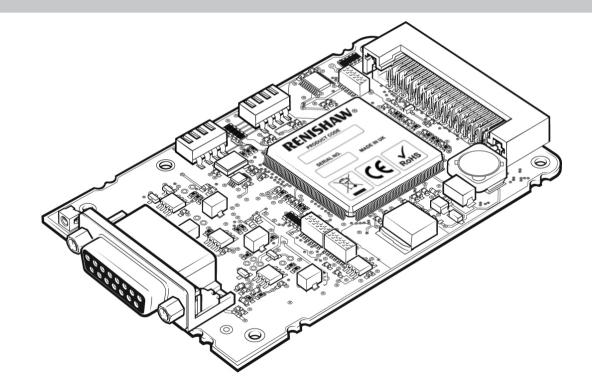
**User's guide** M-9904-2254-06-A



# **RPI20** parallel interface



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Renishaw part no: M-9904-2254-06-A

Issued: 08 2017

#### Care of equipment

The RPI20 parallel interface contains precision electronic components. Avoid exposure to moisture. Remove power before connecting, disconnecting, handling or changing switch settings.



**WARNING:** Use correct handling techniques when touching any of the RPI20 assemblies to prevent damage from electrostatic discharge (ESD).

#### **Changes to Renishaw products**

Renishaw plc reserves the right to improve, change or modify its products and documentation without incurring any obligation to make changes to Renishaw equipment previously sold or distributed.

#### Warranty

Renishaw plc warrants its equipment provided that it is installed exactly as defined in associated Renishaw documentation.

#### Safety

It is the responsibility of the manufacturer and/or encoder system installation authority to ensure that, in safety critical applications of the RPI20 parallel interface, any form of signal deviation from the limits of the receiving electronics, howsoever caused, shall not cause the machine to become unsafe. It is also their responsibility to ensure that the end user is made aware of any hazards involved in the operation of their machine, including those mentioned in Renishaw product documentation, and to ensure that adequate guards and safety interlocks are provided.

When using the RPI20 as part of a positioning system on machines, beware of pinch and/or crush hazards that can be created, depending on how and where the equipment is installed.

Further information on safety is contained in Appendix B.

The RPI20 has been designed for use with an RLE laser encoder only. Its use is not supported with other encoder systems.

## **FCC** notice

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

The user is cautioned that any changes or modifications not expressly approved by Renishaw plc or authorised representative could void the user's authority to operate the equipment.

#### **EC** compliance

CE

Renishaw plc declares that the RPI20 parallel interface and VME host PCB comply with the applicable directives, standards and regulations. A copy of the full EC Declaration of Conformity is available at the following address:

## WEEE



The use of this symbol on Renishaw products and/or accompanying documentation indicates that the product should not be mixed with general household waste upon disposal. It is the responsibility of the end user to dispose of this product at a designated collection point for waste electrical and electronic equipment (WEEE) to enable reuse or recycling. Correct disposal of this product will help to save valuable resources and prevent potential negative effects on the environment. For more information, please contact your local waste disposal service or Renishaw distributor.

## **Packing material information**

Complient with EC directive 2011/65/EU (RoHS)

Packaging component	Material	ISO 11469	Recycling guidance
Outer box	Cardboard	n/a	Recyclable
Inserts	Low Density Polyurethane Foam	LDPU	Recyclable
Bags	Low Density Polyethylene	LDPE	Recyclable

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# 1 System overview

The RPI20 converts 1 Vpp analogue quadrature signals from an RLE laser interferometer encoder system into a position reading, which is available over a parallel bus. A typical system set-up, showing two RPI20s mounted in a VME host PCB, is shown in Figure 1.

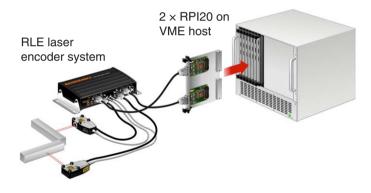


Figure 1 – Typical RPI20 set-up

The RPI20 gives an output of both axis position and status over a TTL compatible bus. The position is available as a 36-bit two's complement word, with a choice of least significant bit (LSB) resolution. The status information includes the signal strength and error flags.

The RPI20 has eight DIP switches which are used for configuration. Three are allocated to set up a unique base address allowing up to seven RPI20s to be used on one common bus. The others allow the RPI20 output to be configured. An individual RPI20 is shown in Figure 2.

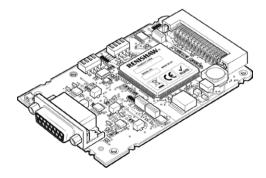


Figure 2 – RPI20 parallel interface

2

A VME host PCB is available to mount one or two RPI20s in one 6U size VME card. More information on this is given in Appendix D.

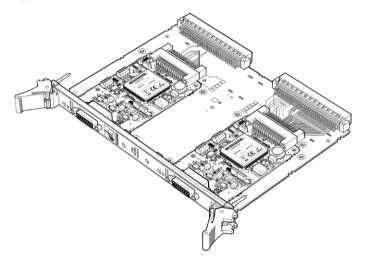
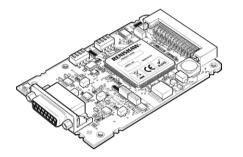


Figure 3 – Two RPI20s in a VME host PCB

#### Part numbers

The following saleable part numbers are available:

• RPI20-P9-XX RPI20 parallel interface (90° connector)



A-9904-2255 RPI20 VME host PCB

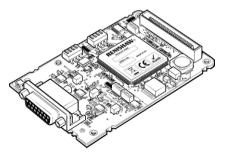
**Note:** The RPI20 VME host PCB is compatible only with the 90° connector version of the RPI20.

In addition, the mating half of the RPI20 parallel bus connectors can also be supplied by Renishaw. The saleable part numbers are:

- A-9904-2256 RPI20 connector 0°
- A-9904-2257 RPI20 connector 90°

For information on these connectors please refer to Appendix C.

RPI20-P0-XX RPI20 parallel interface (0° connector)



# 2 Installation

The RPI20 may be installed either as a stand-alone assembly or in a VME host PCB. This section details the common installation requirements for both assemblies.

Specific installation details for the stand-alone RPI20 are detailed in Appendix C.

Specific installation details for using the RPI20 in a host VME PCB are detailed in Appendix D.

**WARNING:** Do not adjust any of the potentiometers on the RPI20. These have been factory set for optimum performance. Adjusting the potentiometers may degrade system performance and may prevent reliable detection of input signal (sine/cosine) failure, leading to incorrect position data.

# 2.1 Handling precautions

**WARNING:** Use correct handling techniques when touching any of the RPI20 assemblies to prevent damage from ESD.

## 2.2 Analogue quadrature interface

The RPI20 accepts the nominal 1 Vpp analogue quadrature from the RLE. Signal termination is contained within the RPI20 itself. There is no need for any other termination to be used.

## Cabling

The choice of cables for this application is very important. A cable with individually screened twisted pairs is recommended. An example of a suitable cable is the Belden 8164 cable. The maximum recommended cable length is 10 m.

The signals should be wired as shown in Table 1:

Table 1 – Signal wiring between RLE and F
---

Signal	Function
1st pair	Sine and /Sine
2nd pair	Cosine and /Cosine
3rd pair	Error and /Error
Individual screens	0 V (both ends)
Outer screen	Case/shell (both ends)

**WARNING:** It is essential that the error line inputs are connected so that the RPI20 can determine if any errors have occurred in the RLE system. If the analogue quadrature is incorrectly wired, the system may still work but may move distances and at speeds that are not expected and may move in the opposite direction to that expected. If a voltage exceeding  $\pm 7$  V is applied on any of the signals, damage to the unit can occur.

**WARNING:** Care should be taken to ensure that individual signal wires do not short. It is advised that all joints are sleeved. If input signal wires short, the position output will be unreliable and the error signal may not work reliably.

#### **Connector pin out**

The analogue quadrature input connector pin out is shown in Table 2. All pins are protected to  $\pm 7$  V. The connector on the RPI20 is a 15 way female D-type. Figure 4 shows the mating D-type connector.

Pin number	Function
1	0 V
2	-
3	Error
4	_
5	Sine
6	Cosine
7	-
8	-
9	-
10	/Error
11	-
12	/Sine
13	/Cosine
14	-
15	-
Shell	Chassis ground

Table 2 – An	nalogue q	uadrature i	input (1	5 way	D-type	male)
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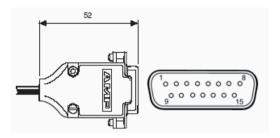


Figure 4 – Analogue quadrature input mating connector (15 way D-type male connector)

## 2.3 Parallel bus interface

Specific backplane requirements for the stand-alone RPI20 are detailed in Appendix C and for the VME-hosted RPI20 in Appendix D. However, the guidelines for getting the best performance from the data bus are the same for the stand-alone RPI20 and the VME-hosted RPI20. This information is given below.

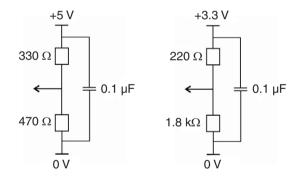
#### General information on the parallel bus

The RPI20 uses TTL bus drivers, which are powered from 3.3 V but are 5 V tolerant. Specifications for IOH and IOL for these drivers are 24 mA. The 74LCX families from Fairchild Semiconductor and Motorola are examples of this type of driver.

To achieve fault free transfer of high-speed signals across the bus, it is recommended that the user follow the guidelines listed in the VME64 specification. These are summarised here.

Termination should be included on the backplane at both ends and the track impedance should be well controlled. This will help to minimise reflections.

A passive or active circuit termination may be used. An example of a passive termination is shown in Figure 5.



#### Figure 5 – Examples of passive bus terminations

The signal bus's track impedance should be kept to nominally 100  $\Omega$  by using Microstrip or Stripline techniques. This will also minimise the cross talk between signals.

# 3 Configuration

## 3.1 RLE set-up – dip switches

If the RPI20 is being used with an RLE system, care should be taken setting the RLE configuration switches correctly.

RLE switch number 5 must be set DOWN to give analogue quadrature output.

RLE switch number 11 must be set DOWN so that the RLE does not tri-state the quadrature on error.

RLE switch number 12 should be set UP unless the fine digital quadrature output from the RLE is also required (in addition to the RPI20 parallel position output).

RLE switch number 13 must be set DOWN so that the RLE does not latch errors. The RPI20 will latch any errors flagged.

**Note:** The RLE axis direction reversal switches 6 and 7 only affect the direction of the digital quadrature from the RLE and not the analogue quadrature.

**Note:** The RLE will flag an error when the measurement velocity reaches a level at which the required output rate of the digital quadrature exceeds the digital bandwidth limit of the RLE. The digital bandwidth limit depends on the digital quadrature resolution and maximum output bandwidth selected with the RLE DIP switches. The digital quadrature resolution and the digital output bandwidth should be selected so that the RLE measurement velocity limit is sufficient for the application. It is therefore recommended that fine quadrature is disabled by setting RLE switch number 12 UP.

For further information on the RLE front panel switches refer to the RLE manual (M-5225-0568).

## 3.2 RPI20 set-up – dip switches

The RPI20 has eight DIP switches which are used to configure the output. The switches are grouped into two banks of four, which are labelled 'SWA' and 'SWB'.

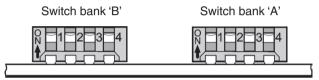


Figure 6 – DIP switch functionality on RPI20

#### Switch A4 – Reserved

This switch is reserved for the sole use of Renishaw plc during manufacture of the equipment. This switch should always be kept in the OFF position.

#### Base address (switches A1, A2 and A3)

These switches are used to configure the base address of the RPI20 parallel interface. The RPI20 may be configured to have a base address between 1 and 7. Base address 0 is reserved for addressing all cards on the same bus simultaneously and so must not be selected. Switch A3 is the most significant bit (MSB) and switch A1 is the least significant bit (LSB), as detailed in Table 3.

**WARNING:** All RPI20 units that are used on the same bus must be configured to have different base addresses. If this is not adhered to, damage may occur to the RPI20 units.

#### Table 3 – Base address select

	Switch		
A1 (LSB)	A2	A3 (MSB)	address
OFF	OFF	OFF	Reserved – do not use
ON	OFF	OFF	1
OFF	ON	OFF	2
ON	ON	OFF	3
OFF	OFF	ON	4
ON	OFF	ON	5
OFF	ON	ON	6
ON	ON	ON	7

## LSB resolution (switches B3 and B4)

Switches B3 and B4 configure the resolution of the LSB of the parallel position word as shown in Table 4.

	Table 4 – LSB resolution select				
Switch		LSB resolution (pm)			
	B3	B4	PMI/DI RLD	RRI RL	

#### Table 4 – LSB resolution select

B3	B4	PMI/DI RLD	RRI RLD
OFF	OFF	38.6	77.2
ON	OFF	77.2	154.4
OFF	ON	154.4	308.8
ON	ON	308.8	617.6

**WARNING:** Care should be taken in configuring these switches when the laser system is used as part of a closed loop system, as an incorrect setting may cause the stage to move further or faster than expected.

**Note:** The LSB resolution is dependent on the type of RLD used as shown in Table 4.

**WARNING:** The position data will roll over when the RPI20 position range limit is exceeded. The stage controller should be programmed to account for this. The RPI20 range varies depending on the LSB resolution selected and the type of RLD used. The values are shown in Table 5.

#### Table 5 – Position range limits

Switch		Range (±m)*		
B3	B4	Plane mirror	Retroreflector	
OFF	OFF	1.3	2.6	
ON	OFF	2.6	5.3	
OFF	ON	5.3	10.6	
ON	ON	10.6	21.2	

\*Actual range achievable will also depend on the laser system used.

#### Axis direction (switch B2)

With the switch in the OFF position and the cosine signal leading the sine signal, the direction of movement is defined as forward and the parallel position will traverse 0x0, 0x1, 0x2, etc.

**WARNING:** It is important to set the direction sense correctly. If it is set incorrectly, the machine will move in the opposite direction to that expected, and may accelerate until it reaches the axis limits. In the case of parallel twin rail drives, it is important that the direction sense of the slave axis is set to match the master axis. Failure to do this will cause opposite ends of the cross-member to move in opposite directions, possibly causing damage to the machine.

## Parity (switch B1)

The parity switch has been included as a safety feature. It prevents the accidental misconfiguration of a single switch. The switch must be used to maintain an even number of switches in the ON position. If this switch is set incorrectly, an error will be asserted and the LED status indicator will be red.

## Factory default switch setting

When initially supplied, the configuration switches are set to a factory default setting as detailed in Table 6.

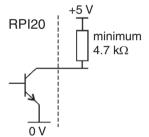
Switch	A1	A2	A3	A4
State	OFF	OFF	OFF	OFF
Switch	B1	B2	B3	B4
State	ON	OFF	OFF	OFF

#### Table 6 – Default setting of configuration switches

**Note:** The factory default switch setting is a non-operational configuration and a parity error will be flagged if the RPI20 is used in this configuration. This is to remind the user that he must configure the RPI20 switch settings before use.

## 3.3 /Error line

The parallel bus includes a /error line which is active low. The / error line indicates if any errors have occurred with either the RLE or the RPI20. The /error line is latched if an error occurs and must be cleared by a reset. The /error line is an open collector output. The signal line should be pulled up to 5 V with a minimum of a 4.7 k $\Omega$  resistor on the backplane as shown in Figure 7.



# 3.4 LED indicator

An LED indicates the status of the RPI20.

#### Table 7 – LED status indicator

LED	Status
Red	RPI20 powered but in error condition
Green	RPI20 powered and no error

#### Figure 7 – Open collector error output wiring

**WARNING:** The open collector /error line is not a failsafe method and therefore additional safety precautions must be taken in safety critical closed loop applications. The /error line must be continually monitored and the motion system must be stopped if it is asserted.

# 4 Communication over the parallel bus

All communication with the RPI20 is performed over the parallel bus. The communication protocol is the same for the stand-alone RPI20 and the VME-hosted RPI20.

Five functions may be performed over the parallel bus:

- 1. Latching all of the RPI20 position and status data simultaneously
- 2. Reading of the latched positions
- 3. Reading of the latched status information
- 4. Resetting of the position and clearing of all errors
- 5. Enabling test information onto the RPI20 parallel bus

All data must be latched before it is read.

## 4.1 Parallel bus

The parallel bus contains a 5-bit address bus, a 36-bit data bus, /enable line and /error line.

## Address bus

The top three lines of the address bus are used to choose which RPI20 unit to communicate with. Each RPI20 unit has a unique base address, selected with DIP switches, as detailed in section 3.2. Base address 0 is reserved for simultaneous communication with all RPI20 units on the bus.

The bottom two lines of the address bus are used to define the required function. The address bus functionality is described in Table 8.

#### Data bus

The RPI20 can be requested to put either position or status data on the data bus. The position data is a 36-bit word with DTA0 as the LSB and DTA35 as the MSB. The status information is detailed in Table 10.

## /Enable

The /enable line has two functions. The first is to latch or reset position and status data. This is initiated by a falling edge of the /enable signal. Secondly, it is used to enable data onto the bus. Refer to Figure 8.

## /Error

The /error line indicates when a fault has occurred in the measurement system. It is described in detail in section 3.3.

## 4.2 Functionality

Five functions may be performed over the parallel bus. These are:

- 1. Resetting the position and error status of the RPI20
- 2. Latching the position and status reading of all RPI20s simultaneously
- 3. Transferring latched position information onto the RPI20 parallel data bus
- 4. Transferring latched status information onto the RPI20 parallel bus
- 5. Transferring test information onto the RPI20 parallel bus

The required function is chosen by selecting the correct register. The functionality is shown in Table 8.

Table 8 – RPI20 address b	ous functionality
---------------------------	-------------------

RPI20	Ad	dress	ess location (bit)			Pagiatar	Function			
RPI20	4	3	2	1	0	Register	Function			
				0	0	1	Latch all RPI20 units			
All	0			0	1	2	Reserved			
All	0	0	0	1	0	3	Reset all RPI20 units			
				1	1	4	Reserved			
				0	0	1	Read RPI20 unit 1 position			
Unit 1	0			0	1	2	Read RPI20 unit 1 status			
	Init 1 0 0		1	1	0	3	RPI20 unit 1 reset			
				1	1	4	Read RPI20 unit 1 test information			
		0 1		0	1	Read RPI20 unit 2 position				
Unit 2	0			0	1	2	Read RPI20 unit 2 status			
Unit 2	0	1		I	0	0	1	0	3	RPI20 unit 2 reset
				1	1	4	Read RPI20 unit 2 test information			
				0	0	1	Read RPI20 unit 7 position			
	Unit 7 1 1 1 0 1			0	1	2	Read RPI20 unit 7 status			
			3	RPI20 unit 7 reset						
				1	1	4	Read RPI20 unit 7 test information			

#### Reset

Register 3 is used to reset the RPI20. If there are no errors currently active in the system, the /error line is reset, any latched error flags are cleared and the position output is set to zero. All RPI20s may be simultaneously reset by addressing register 3 of base address 0 and taking the /enable line low. An individual RPI20 may be reset by addressing register 3 of its base address and taking the /enable line low.

#### Latch data

Register 1 of base address 0 is used to latch both the position data and the status data of all the RPI20s simultaneously.

## Enable position data

Register 1 of a particular RPI20 unit's base address holds the latched position data. If this register is selected on the address bus, then position information is placed on the data bus after the /enable line is taken low. The position output is represented in two's complement format as shown in Table 9.

MSN								LSN	Position
7	F	F	F	F	F	F	F	F	(2 <sup>35</sup> -1 × UOR)
0	0	0	0	0	0	0	0	2	2 × UOR
0	0	0	0	0	0	0	0	1	1 × UOR
0	0	0	0	0	0	0	0	0	0 × UOR
F	F	F	F	F	F	F	F	F	-1 × UOR
F	F	F	F	F	F	F	F	F	-2 × UOR
8	0	0	0	0	0	0	0	0	-2 <sup>35</sup> × UOR

#### Table 9 – Position output in two's complement format

UOR = unit of resolution of LSB as set by switches B1 and B2 MSN = most significant nibble LSN = least significant nibble

#### Enable status data

Register 2 of a particular RPI20 unit holds the latched status information. If this register is selected on the address bus, the status information is placed on the data bus after the /enable line is taken low. Information contained in the status register is detailed in Table 10.

Table 10 – Status	information
-------------------	-------------

Bits	Function	Comment			
0-9	Analogue quadrature sample – cosine	This is the digitised input value of the cosine signal *			
10-19	Analogue quadrature sample – sine	This is the digitised input value of the sine signal *			
20-27	Signal level	Amplitude of input quadrature (0 to FF where FF=115% signal strength) *			
28	Encoder error (1 = error)	Error flagged by encoder system			
29	Overspeed error (1 = error)	**			
30	Beam break error (1 = error)	Input quadrature amplitude too low (<12.5%)			
31	Parity error (1 = error)	Parity bit set incorrectly			
32	Switch B3 setting – resolution select	( 1 = ON, 0 = OFF) ***			
33	Switch B4 setting – resolution select	( 1 = ON, 0 = OFF) ***			
34	Switch B2 setting – direction select	(1 = REV, 0 = FWD) ***			
35	Reserved				

\* Bits 0, 10, 20 are the LSBs of the digitised cosine, sine and signal level values respectively.

- \*\* An overspeed error is flagged when the input analogue quadrature rate exceeds the processing capability of the RPI20.
- \*\*\* Inclusion of switch settings B2, B3, B4 in the status word allows the host system to check that the resolution and direction sense are correctly set before enabling motion.

#### Enable test data

Register 4 of a particular RPI20 unit holds test information which can be used for checking the data bus for open and short circuits and failed drivers. The information held in the test register depends on the status of the parity switches as shown in Table 11.

#### Table 11 – Test information

Parity switch	Test register output
Even combination	AAAAAAAA (hex A = '1010')
Odd combination	55555555555555 (hex 5 = '0101')

**Note:** The test information in register 4 may be used to verify the presence of all expected RPI20s at power-up and before engaging drives.

## 4.3 Timing diagram

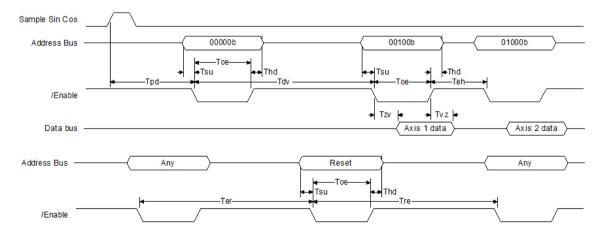
A timing diagram for a two-axis position read is shown below. The read consists of three separate stages.

- Latch data by asserting /enable with the address but set to 00000b (base address 0, register 1) \*
- 2. Read in position data from axis 1 by taking /enable low whilst the address bus is set to 00100b (base address 1, register 1) \*\*
- Read in position data from axis 2 by taking /enable low whilst the address bus is set to 01000b (base address 2, register 1) \*\*

The same timing sequence should be used to reset an RPI20.

**Note:** A delay of Tdv should be left before reading back the reset position.

- This will replace any previously latched data.
- \*\* This will not clear the latched position. It can be read again if necessary.



Parameter	Min	Nom	Max	Units	Comment			
Tsu	10			ns	Set-up of address before /Enable falling edge			
Тое	50			ns	Minimum period that /Enable must be active			
Thd	10			ns	Period address to be held after /Enable rising edge			
Tzv			35	ns	/Enable to data valid			
Tvz			35	ns	Data valid to hi-impedance state			
Tpd	70	80	90	ns	Propagation delay. The time before the /Enable that the position event occurred. This defines the delay due to RPI20 only.			
Tdv	140	150	160	ns	Delay between /Enable falling edge and valid position.			
Tsp	100			ns	Time between sequential axis access			
Teh	50			ns	Minimum period that /Enable must be high			
Ter	140			ns	Minimum delay from /Enable falling edge of previous bus access and reset			
Tre	160			ns	Minimum delay between /Enable falling edge of reset and next bus access			

Table 12 – Timing parameters

Based on these timings, the maximum update rates for reading the position information depends on the number of axes to be read in sequence, as shown in Appendix A, Table 13.

# Appendix A – Specification

Values in this table define the contribution of the RPI20 on the system performance, NOT the complete laser interferometer system performance.

#### Table 13 – Measurement performance

			PMI	RRI	
LSB resolutio	on – user s	38.6, 77.2,77.2,154.4154.4 or308.8 or308.8 pm617.6 pm			
Maximum spe	ed		1 m/s	2 m/s	
Positional no	ise contrib	ution (RMS)	< 38 pm	< 77 pm	
SDE	Velocity	< 50 mm/s (PMI) < 100 mm/s (RRI)	< ±0.5 nm	< ±1 nm	
contribution	Signal st	rength > 70% and < 120%			
	Velocity	Velocity > 50 mm/s and < 1 m/s (PMI) > 100 mm/s and < 2 m/s (RRI)		< ±4 nm	
Position data	format		36-bit (two's complement)		
Propagation of before latch e		al position is sampled al)	80 ns		
Propagation of	delay varia	tion	±10 ns		
	1 axis sy	stem	4 MHz		
Massimosom	2 axis sy	2.86 MHz			
Maximum update rate	3 axis sy	2.22 MHz			
	Multi-axis	s system	Each extra axis requires an extra 100 ns to read		

#### Table 14 – RPI20 power requirement

Voltage	5 V ±0.25 V				
Operating current	0.5 A				
Noise and ripple	50 mVpp (DC to 10 MHz)				

The 5 V power supply should be single fault tolerant certified to EN (IEC) 60950-1.

#### Table 15 – Environmental specification

Pressure	Normal atmospheric (650 mbar – 1150 mbar)				
Humidity	0-95% RH (non-condensing)				
Tomporatura	Storage	-20 °C to +70 °C			
Temperature	Operating	+10 °C to +40 °C			

# Appendix B – Safety information

#### General

The RPI20 is designed for integration into the primary position feedback loop of a motion system. It is essential that the system is installed in accordance with the instructions in the installation manuals. It is the responsibility of the system integrator to ensure that, in the event of a failure of any part of the RPI20, the motion system remains safe.

In motion systems with powers or speeds capable of causing injury, safety protection measures must be included in the design. It is recommended that satisfactory operation of these protection measures is verified **before** the feedback loop is closed. The following are examples of safety protection measures that can be used. It is the sole responsibility of the system integrator to select appropriate measures for their application.

- 1. The RPI20 includes an error signal output. The control system must be designed to stop the axis motion if this error is asserted.
- 2. The axis must include physical limit switches which, when tripped, will stop axis motion before damage occurs (soft limits alone are insufficient).

- 3. Motor torque monitoring. If the motor torque exceeds an expected limit, the axis of motion must be stopped.
- 4. The machine must include an emergency stop button.
- Following error detection, if the difference between the controller demand position and the axis feedback position exceeds an expected limit, the axis motion must be stopped.
- 6. Guards, viewing windows, covers and interlocks may be used to prevent user access to hazardous areas, and to contain ejected parts and materials.
- If the machine includes an independent tacho (velocity) feedback system, this should be cross-checked with the position feedback. For example, if the tacho indicates the axis is moving, but the position feedback doesn't, the axis motion must be stopped.
- 8. In the case of synchronised parallel motion systems (for example twin rail gantry drive systems), the relative positions of master and slave axes should be monitored. If the difference in their positions exceeds an expected limit, axis motion must be stopped.

For further advice, consult the appropriate machinery safety standards.

#### LSB resolution

It is important to set the LSB resolution of the RPI20 correctly. If the LSB resolution is set incorrectly, the axis may move for distances and at speeds that are not expected.

#### **Direction sense**

It is important to set the direction sense correctly. If it is set incorrectly, the machine will move in the opposite direction to that expected, and may accelerate until it reaches the axis limits. In the case of parallel twin rail drives, it is important that the direction sense of the slave axis is set to match the master axis. Failure to do this will cause opposite ends of the cross-member to move in opposite directions, possibly causing damage to the machine.

#### /Error signal monitoring

The RPI20 parallel interface continuously checks for internal errors and errors in the encoder system that may cause invalid position feedback signals, and signals a fault by asserting an / error line output. In the case of closed loop motion systems, for safe operation the status of this /error line must be monitored. If the /error line goes low, the position feedback signals may be incorrect and the axis of motion must be stopped.

#### Power supply out of range

The correct power supply voltage is 5 V  $\pm$ 0.25 V. Power supplies outside of this range may give unreliable operation or damage the RPI20 unit.

#### Position data integrity

If an error is signalled by the RPI20, then the RPI20 position data may be incorrect. The system must be reset and re-referenced before it is used for position feedback again.

# Appendix C – Stand-alone installation of the RPI20

The RPI20 can be supported using the four mounting holes (A, B, C and D) which are suitable for M3 screws. The position of the holes for both RPI20 variants is shown in Figures 9 and 10. All dimensions are in millimetres.

**Note:** Holes A and B are electrically connected to chassis ground. Holes C and D are unconnected.

**Note:** Mounting screws should not exceed a maximum torque of 0.6 nm.

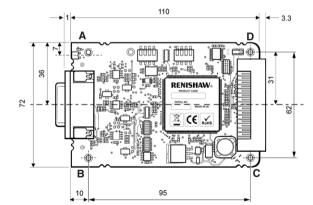


Figure 9 – RPI20-P9-XX

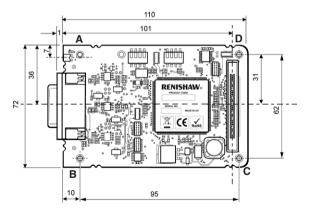


Figure 10 – RPI20-P0-XX

#### Connector

The correct mating connectors for the RPI20 parallel bus are the JAE TX24 60R family of connectors. These may be supplied by Renishaw or direct from JAE.

Table 16 – RPI20 parallel bus connector pin out

						-			
Pin	Label	Pin	Label		Pin	Label		Pin	Label
1	5 V	16	DTA26		31	5 V		46	DTA19
2	0 V	17	DTA25		32	0 V		47	DTA18
3	DTA15	18	DTA24		33	DTA7		48	DTA17
4	DTA14	19	DTA33		34	DTA6		49	DTA16
5	DTA13	20	DTA32		35	DTA5	]	50	DTA35
6	DTA12	21	DTA34		36	DTA4	]	51	Reserve
7	DTA11	22	Reserved		37	DTA3	]	52	Reserve
8	DTA10	23	Reserved		38	DTA2	1	53	Reserve
9	DTA9	24	ADD4		39	DTA1	1	54	Reserve
10	DTA8	25	ADD3		40	DTA0	1	55	Reserve
11	DTA31	26	ADD2		41	DTA23	1	56	Reserve
12	DTA30	27	ADD1		42	DTA22		57	Reserve
13	DTA29	28	ADD0		43	DTA21	1	58	/Enable
14	/Error (O/C)	29	0 V		44	DTA20	]	59	0 V
15	DTA27	30	5 V	1	45	DTA28	1	60	5 V

Note: The reserved pins should be left unconnected.

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 Table 17 – Part numbers for JAE connectors

Description	Renishaw part number	JAE part number
RPI20 mating 0° connector	A-9904-2256	TX24-60R-6ST-H1E
RPI20 mating 90° connector	A-9904-2257	TX24-60R-LT-H1E

**Note:** using RPI20 mating 0° connector, A-9904-2256, separation between boards = 12 mm

Figure 11 – RPI20 parallel bus mating connector (LT and ST variants)

Other separations can be achieved using other receptacles.

For detailed information on the connectors, please visit the JAE web site at:

www.jae-connector.com

# Appendix D – VME-hosted RPI20 installation

The VME host PCB is compatible with a 6U size VME rack. All communication is performed using the P2 bus. No communication is available over the P1 bus. Either the P1 or P2 bus may be used to power the RPI20.

The VME P2 bus should be terminated at both ends of the backplane in accordance with the VME specification.

It is recommended that, in applications requiring three or more axes, VME-hosted RPI20s should be mounted in adjacent slots in the VME rack.

## VME host PCB connector pin outs

The pin outs for the P1 and P2 connectors are shown in Tables 17 and 18.

Table 18 – VME P1 bus connector pin out

Pin	Row A	Row B	Row C	Pin	Row A	Row B	Row C
1	-	-	-	17	0 V	-	-
2	-	-	-	18	-	-	-
3	-	-	-	19	0 V	-	-
4	-	-	-	20	-	0 V	-
5	-	-	-	21	-	-	-
6	-	-	-	22	-	-	-
7	-	-	-	23	-	0 V	-
8	-	-	_	24	-	-	-
9	0 V	-	0 V	25	-	-	-
10	-	-	-	26	-	-	-
11	0 V	-	-	27	-	-	-
12	-	-	-	28	-	-	-
13	-	-	-	29	-	-	-
14	-	-	-	30	-	-	-
15	0 V	-	-	31	-	-	-
16	-	_	-	32	+5 V	+5 V	+5 V

Table 19 – VME P2 bus connector pin out

Pin	Row A	Row B	Row C
1	/Enable	+5 V	-
2	0 V	0 V	0 V
3	ADD00	-	-
4	ADD01	-	-
5	ADD02	-	-
6	ADD03	-	/Error (O/C)
7	ADD04	-	-
8	Reserved	-	-
9	-	-	-
10	-	-	-
11	0 V	-	0 V
12	DTA32	0 V	DTA34
13	DTA33	+5 V	DTA35
14	0 V	-	0 V
15	DTA16	-	DTA24
16	DTA17	-	DTA25

Pin	Row A	Row B	Row C	
17	DTA18	-	DTA26	
18	DTA19	-	DTA27	
19	DTA20	-	DTA28	
20	DTA21	-	DTA29	
21	DTA22	-	DTA30	
22	DTA23	0 V	DTA31	
23	DTA00	-	DTA08	
24	DTA01	-	DTA09	
25	DTA02	-	DTA10	
26	DTA03	-	DTA11	
27	DTA04	-	DTA12	
28	DTA05	-	DTA13	
29	DTA06	-	DTA14	
30	DTA07	-	DTA15	
31	0 V	0 V	0 V	
32	-	+5 V	-	

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